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BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, IL 60610

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,308	NAJAM ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-41 have been examined.

Papers Received

2. Receipt is acknowledged of the amendment papers submitted where the papers have been placed of record in the file.

3. The objections to the abstract and drawings have overcome by the amendment and are herein withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8-9,11-15,18,19,22-28,31,34-36, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rutman (patent No. 5,313,586) in view of Olgiati (European patent application EP1061439A1 published 12/20/2000).

In regard to claim 1 Rutman discloses a packet processing system comprising:

a. a processor figure 3, element 270);

b. a co-processor (figure 3, element 260) separated from said processor by a boundary; [Column 4, lines 24-26 explicitly shows that element 260 is in fact a co-processor. The figure shows a boundary between the processor and co-processor in being all the space between the two processor.]

c. and an interface (figure 3, elements 200,280,340, and 350) coupled with said processor and said co-processor and operative to bridge said boundary,

d. said interface including :

i. a memory coupled with said processor and said co-processor (figure3, element 200, VRAM) said memory having at least two read/write ports for reading and writing data to said memory (figure 3, A and B) wherein said processor is coupled with one of said at least two ports; [Figure 3 shows that the processor (P1) is coupled to port A of the memory and the co-processor (P2) is coupled to port B. Column 4, lines 22-23, shows that these blocks, A (220) and B (210), are in fact ports (serial ports) of the VRAM memory.]

ii. and control logic coupled with said at least two read/write ports (figure 3, elements 280,340 and 350); Column 4, lines 26-28 show that arbitration is performed to determine which port has access to the memory and thus the arbiter (280) is coupled to the ports. In addition, column 4, lines 38-41, show that P2 CTL (340) generates memory requests for the arbiter, P1 CTL (350) and P2 CTL (340) are both shown in the figure to be coupled to the arbiter and thus are also indirectly coupled to the ports.]

e. wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor; said co-processor stores data intended for said processor to said memory and read data stored by said processor from said memory independent of said

processor [Column 3, lines 15-34 show that the memory is used for communication between processors as storage independent from the processors where data intended for the other processor is transferred when needed since communication is usually not immediately required. Column 3, lines 47-53 show that this communication is between a processor and coprocessor. In the embodiment of figure 3, the communication is also between the processor and coprocessor.]

f. and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; [As shown above, the control logic generates memory control signals and requests, which facilitate the reading of stored data during the communication between the processors.]

g. and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously . [The term " substantially simultaneously is a very broad term that means "about the same time" which the Examiner is interpreting to be within a cycle of one another (though the interpretation could be even broader). With this interpretation, as Applicant pointed out, the co-processor communication with memory is only interrupted when the processor communicates via the serial port. Thus the processor is capable of storing to the memory on the serial port the cycle after the co-processor had been storing to the memory on the random access port.]

Rutman did not disclose (claims 1,11, 24, and 34) wherein each of said processor and said coprocessor is capable of accessing said memory without preventing access by the other of said processor and co-processor. Olgiati however

taught an interface between a processor and coprocessor (e.g., see fig. 1) that provided burst communications that decouples the operation of the processor and coprocessor (e.g., see paragraph 0016) and double buffering or having the processor and coprocessor write to different regions of memory decoupling the operation of the processor and coprocessor including with respect to access to the memory (e.g. see paragraphs 0020-0024). The storeburst and loadburst instructions complete in a single cycle (e.g., see paragraphs 0031-0034). This clearly provides for a system where each the processor and coprocessor is capable of accessing the memory without preventing access by the other of the processor and co-processor.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the Rutman system to incorporate the burst synchronous transfer at least to provide faster transfer of data eliminate waiting for access to memory.

4. In regard to claim 2, Rutman discloses the packet processing system of claim 1, wherein said boundary comprises a printed circuit board-to-printed circuit board connector coupled between said processor and said co-processor. [Column 1, lines 23-25 show that the shared memory is a separate entity. With the memory being on a separate chip or circuit board and the processor and co-processor communicating via serial ports, as shown previously, the use of a circuit board to circuit board connector in the form of a serial connector or cable must be used to coupled the processor and co-processor to the memory. Since the processor and co-processor are coupled to the same memory, they are also coupled to each other.]

5. In regard to claim 3, Rutman discloses the packet processing system of claim 1, wherein said processor communicates with a first protocol and said co-processor communicates with a second protocol, said boundary comprising a difference between said first and second protocols, said interface being further operative to translate data between said first ant second protocols. [The previously enclosed second IEEE definition of "protocol" shows that a protocol includes conventions governing the format of message exchange between two communication terminals. As shown above, the processor and co-processor of Rutman communicate and are thus communication terminals; Column 5, lines 54-58 show that the processor and coprocessor operate with different bus widths. This means that the format of any communication or message exchange between the processor and coprocessor will be initially be of a different format and thus the processor and co-processor communicate with different protocols. Since Rutman discloses the ability of communication between a processor and coprocessor of different widths, he inherently includes as part of the interface a means for compromising the two protocols so that communication can occur.]

6. In regard to claim 4, Rutman discloses the packet processing system of claim 1, wherein said processor is a network processor. [The previously included IEEE definition of "network" as it pertains to data transmission is a series of points interconnected by communication channels. Since the processor (one point) is communicating with the co-processor (the second point) as shown above, the processor is communicating over a network and is thus a network processor.]

7. In regard to claim 5, Rutman discloses the packet processing system of claim 1, wherein said co-processor is a task specific processor. [Figure 3 shows that the co-processor (P2) is a graphics accelerator, thus performing the specific task of graphics acceleration.]

8. In regard to claim 8, Rutman discloses the packet processing system of claim 1, wherein said control logic signals said processor when said co-processor has stored data to said memory. As shown above, the control logic sends signals to the memory and processor for their interaction. [Column 1, lines 23-28 show that polling or interrupts are used in each processor so that each processor knows when data to be accessed is placed in the shared memory.]

9. In regard to claim 9, Rutman discloses the packet processing system of claim 1, wherein said control logic signals said co-processor when said processor has written data to said memory. [As shown above, the control logic sends signals to the memory and processor for their interaction. Column 1, lines 23-28 show that polling or interrupts are used in each processor so that each processor knows when data to be accessed is placed in the shared memory.]

10. In regard to claim 11, Rutman discloses an interface (figure 3 elements 200,280,340, and 350) for coupling a processor (element 270) to a co-processor (element 260) said interface comprising:

i. a memory coupled with said processor and said co-processor (figure 3, element 200, VRAM) said memory having at least two read/write ports for reading and writing data to said memory (figure 3, A and B) wherein said processor is

coupled with one of said at least two ports; [Figure 3 shows that the processor (P1) is coupled to port A of the memory and the co-processor (P2) is coupled to port B. Column 4, lines 22-23, shows that these blocks, A (220) and B (210), are in fact ports (serial ports) of the VRAM memory.]

ii. and control logic coupled with said at least two read/write ports (figure 3, elements 280,340 and 350); Column 4, lines 26-28 show that arbitration is performed to determine which port has access to the memory and thus the arbiter (280) is coupled to the ports. In addition, column 4, lines 38-41, show that P2 CTL (340) generates memory requests for the arbiter, P1 CTL (350) and P2 CTL (340) are both shown in the figure to be coupled to the arbiter and thus are also indirectly coupled to the ports.]

c. wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor; said co-processor stores data intended for said processor to said memory and read data stored by said processor from said memory independent of said processor [Column 3, lines 15-34 show that the memory is used for communication between processors as storage independent from the processors where data intended for the other processor is transferred when needed since communication is usually not immediately required. Column 3, lines 47-53 show that this communication is between a processor and coprocessor. In the embodiment of figure 3, the communication is also between the processor and coprocessor.]

d. and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; [As shown above, the control logic generates memory control signals and requests, which facilitate the reading of stored data during the communication between the processors.]

e. and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously . [The term " substantially simultaneously is a very broad term that means "about the same time" which the Examiner is interpreting to be within a cycle of one another (though the interpretation could be even broader). With this interpretation, as Applicant pointed out, the co-processor communication with memory is only interrupted when the processor communicates via the serial port. Thus the processor is capable of storing to the memory on the serial port the cycle after the co-processor had been storing to the memory on the random access port.]

11. In regard to claim 12, Rutman discloses the interface of claim 11, wherein said boundary comprises a printed circuit board-to-printed circuit board connector coupled between said processor and said co-processor. [Column 1, lines 23-25 show that the shared memory is a separate entity. With the memory being on a separate chip or circuit board and the processor and co-processor communicating via serial ports, as shown previously, the use of a circuit board to circuit board connector in the form of a serial connector or cable must be used to coupled the processor and co-processor to the memory. Since the processor and co-processor are coupled to the same memory, they are also coupled to each other.]

12. In regard to claim 13, Rutman discloses the interface of claim 11, wherein said processor communicates with a first protocol and said co-processor communicates with a second protocol, said boundary comprising a difference between said first and second protocols, said interface being further operative to translate data between said first ant second protocols. [The previously enclosed second IEEE definition of "protocol" shows that a protocol includes conventions governing the format of message exchange between two communication terminals. As shown above, the processor and co-processor of Rutman communicate and are thus communication terminals.Column 5, lines 54-58 show that the processor and coprocessor operate with different bus widths. This means that the format of any communication or message exchange between the processor and coprocessor will be initially be of a different format and thus the processor and co-processor communicate with different protocols. Since Rutman discloses the ability of communication between a processor and coprocessor of different widths, he inherently includes as part of the interface a means for compromising the two protocols so that communication can occur.]

13. In regard to claim 14, Rutman discloses the interface of claim 11 wherein said processor is a network processor. [The previously included IEEE definition of "network" as it pertains to data transmission is a series of points interconnected by communication channels. Since the processor (one point) is communicating with the co-processor (the second point) as shown above, the processor is communicating over a network and is thus a network processor.]

14. In regard to claim 15 Rutman discloses the interface of claim 11wherein said co-processor is a task specific processor. [Figure 3 shows that the co-processor (P2) is a graphics accelerator, thus performing the specific task of graphics acceleration.]

15. In regard to claim 18, Rutman discloses the interface of claim 11, wherein said control logic signals said processor when said co-processor has stored data to said memory. As shown above, the control logic sends signals to the memory and processor for their interaction. [Column 1, lines 23-28 show that polling or interrupts are used in each processor so that each processor knows when data to be accessed is placed in the shared memory.]

16. In regard to claim 19, Rutman discloses the interface of claim 11, In regard to wherein said control logic signals said processor when said co-processor has written data to said memory. [As shown above, the control logic sends signals to the memory and processor for their interaction. Column 1, lines 23-28 show that polling or interrupts are used in each processor so that each processor knows when data to be accessed is placed in the shared memory.]

17. In regard to claim 22, Rutman discloses the interface of claim 11, wherein said interface allows said processor to operate independently of the interface requirements of said co-processor. [As shown above, the communication (an operation) between the processor and co-processor is made independent by use of the shared memory that is accessed when data is needed.]

18. In regard to claim 23, Rutman discloses the interface of claim 11, processor is located on a first circuit board and said co-processor is located on a second circuit

board coupled with said first circuit board by a first connector, said first connector characterized by at least one electrical characteristic, said interface operative to isolate said processor and said co-processor from said at least one electrical characteristic. [Column 5, line 54-58 show that the processor an co-processor have different bus sizes. With the two processors having different widths, they cannot be on the same circuit since every connection to each processor is of different length. As shown above, th processor and co-processor are each coupled to the memory by serial ports and thus to each other using a first connect from the processor and a second connector from the co-processor. Due to the different sizes, the processor and co-processor are connected to the memory with connectors that each have different electrical characteristics due to the inherently different effective connector widths. Since the interface connects the processor and co-processor it inherently isolates the different electrical characteristics of the connectors so that communication can occur.]

19. In regard to claim 24, Rutman disclosed a method of interfacing a processor (figure 3, P1) with a co-processor (P2) across a boundary, said processor and said co-processor being separated by said boundary, said method comprising:

(a) receiving first data from said processor via a first interface

(b) storing said first data in a memory;

(c) signaling said co-processor that said first data has been stored;

(d) receiving a read command from said co-processor via a second interface;

(e) providing said first data to said co-processor via said second interface across said boundary;

wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously.

[Figure 3 shows that the processor (P1) is coupled to a port (a first interface of the memory and the co-processor is (P2) is coupled to port B (a second interface of the VRAM memory. Column 3, lines 15-34 show that the memory is used for communication between processors as storage independent from the processors where data intended for the other processor is transferred when needed since communication is usually not immediately required. Column 3, lines 47-53 show that this communication is between a processor and coprocessor. In the embodiment of figure 3, the communication is also between the processor and coprocessor. Column 4, lines 26-28 show that arbitration is performed to determine which port has access to the memory and thus the arbiter (280) is coupled to the ports. In additions column 4, lines 38-41 show that P2 CTL (340) generates memory control signals and column 5, lines 5-8 show that P1 CTL (350) generates memory requests (read requests or commands) for the arbiter. P1 CTL (350) and P2 CTL (340) are both shown in the figure to be coupled to the arbiter and thus are also indirectly coupled to the ports. This control logic generates memory control signals and requests, which facilitate the reading of stored data during the communication between processors. Column 1, lines 23-28 show that polling or interrupts are used in each processor so that each processor knows when data to be accessed is placed or stored in the shared memory. [The term " substantially simultaneously is a very broad term that means "about the same time" which the Examiner is interpreting to be within a cycle of one another

(though the interpretation could be even broader). With this interpretation, as Applicant pointed out, the co-processor communication with memory is only interrupted when the processor communicates via the serial port. Thus the processor is capable of storing to the memory on the serial port the cycle after the co-processor had been storing to the memory on the random access port.]

1. In regard to claim 25 Rutman discloses the method of claim 24, further comprising:

(a) receiving second data from said processor via a second interface

(b) storing said second data in said memory;

(c) signaling said processor that said second data has been stored;

(d) receiving a read command from said processor via a first interface;

(e) providing said second data to said processor via said first interface across said boundary;

[The above method functionality is shown to work for communication by both the processor and co-processor and thus the argument fits the limitations of this claim as well.]

20. In regard to claim 26 Rutman discloses the method of claim 24 , wherein said providing further comprises providing said first data across a boundary comprising a printed circuit board-to-printed circuit board connector [Column 1, lines 23-25 show that the shared memory is a separate entity. With the memory being on a separate chip or circuit board and the processor and co-processor communicating via serial ports, as shown previously, the use of a circuit board to circuit board connector in the form of a

serial connector or cable must be used to coupled the processor and co-processor to the memory.]

21. In regard to claim 27 Rutman discloses the method of claim 24, said method further comprising using a network processor as said processor [The previously included IEEE definition of "network" as it pertains to data transmission is a series of points interconnected by communication channels. Since the processor (one point) is communicating with the co-processor (the second point) as shown above, the processor is communicating over a network and is thus a network processor.]

22. In regard to claim 28, Rutman discloses the method of claim 24, said method comprising using a task specific processor as said co-processor. [Figure shows that the co-processor (P2) is a graphics accelerator, thus performing the specific task of graphics acceleration.]

23. In regard to claim 31 Rutman discloses the method of claim 24, wherein said signaling is performed by control logic signal coupled with said memory. [As shown above, figure 3 shows the stated the control logic that performs signaling is coupled to the memory.]

24. In regard to claim 34, Rutman discloses an apparatus for facilitating communications between a first processor (figure, element 270) and a second processor (element 260), the apparatus comprising:

a. a dual port memory (figure 3, element 200) coupled with said first processor via first interface (element B) and said second processors via a second interface (element A) and operative to act as a message buffer between said first

processor and said second processor; [Figure 2 shows the memory is a 3-port VRAM with dual serial ports (A and B to serial 1 and serial 2). Column 3, lines 15-34 show that the memory is used for communication between processors as storage independent from the processors where data intended for the other processor is transferred when needed since communication is usually not immediately required.]

b. and control logic coupled with said dual ported memory and operative to detect communications by one of said first and second processors and inform the other of said first and second processors and said communications; [Column 4, lines 26-28 show that arbitration is performed to determine which port has access to the memory and thus the arbiter (280) is coupled to the ports. . In addition column 4, lines 38-41 show that P2 CTL (340) generates memory control signals and column 5, lines 5-8 show that P1 CTL (350) generates memory requests (read requests or commands) for the arbiter. P1 CTL (350) and P2 CTL (340) are both shown in the figure to be coupled to the arbiter and thus are also indirectly coupled to the ports. This control logic generates memory control signals and requests, which facilitate the reading of stored data during the communication between processors. Column 1, lines 23-28 show that polling or interrupts are used in each processor so that each processor knows when data to be accessed is placed or stored in the shared memory.]

c. and wherein said processor and said co-processor are capable or storing data to said memory substantially simultaneously. [The term " substantially simultaneously is a very broad term that means "about the same time" which the Examiner is interpreting to be within a cycle of one another (though the interpretation

could be even broader). With this interpretation, as Applicant pointed out, the co-processor communication with memory is only interrupted when the processor communicates via the serial port. Thus the processor is capable of storing to the memory on the serial port the cycle after the co-processor had been storing to the memory on the random access port.]

25. In regard to claim 35, Rutman discloses the apparatus of claim 34, wherein said first processor comprises a network processor. . [The previously included IEEE definition of "network" as it pertains to data transmission is a series of points interconnected by communication channels. Since the processor (one point) is communicating with the co-processor (the second point) as shown above, the processor is communicating over a network and is thus a network processor.]

26. In regard to claim 36, Rutman discloses the apparatus of claim 34, wherein said second processor comprises a task specific processor. [Figure 3 shows that the second processor (P2) is a graphics accelerator, thus performing the specific task of graphics acceleration.]

27. In regard to claim 39, Rutman discloses the apparatus of claim 34, control logic signals said first processor when said second processor has written data to said dual ported memory and said control logic signals said second processor when said first processor has written data to said dual ported memory. [As shown above the control logic sends to the memory and processor for their interaction. Column 1, lines 23-28 show that polling or interrupts are used in each processor so that each processor knows when data to be accessed is placed in the shared memory.]

Claims 6,7,16,17,29,30,37,and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rutman and Olgiati as applied to claims 1-5, 8-9,11-15,22-28,31,34-36, and 39 above, and further in view of McCormack (patent No. 5,870,109).

28. In regard to claim 6,

a. Rutman discloses a packet processing system of claim 5, where the coprocessor (P2) is a graphics accelerator as shown in figure 3.

b. Rutman does not disclose wherein said co-processor is a content addressable memory.

c. McCormack has disclosed the use of an overlap detector implemented as a content addressable memory on a graphics accelerator chip (column 3, lines 20-39). Column 2, lines 34-36 show that an object of the invention is to avoid graphic image overlap error in digital imaging, so the overlap detection is needed.

d. McCormack has taught in column 1, lines 41-48 that overlap creates inconsistencies where incorrect data can be used causing an unacceptable error. The detection of overlap so that this error is avoided would have motivated one of ordinary skill in the art to use the overlap detector implemented as a content addressable memory as taught by McCormack in the graphic accelerator co-processor design of Rutman (thus the co-processor "is" the CAM plus other logic, which is allowed due to "is" allowed due to "is" being open ended language as opposed to "consisting of").

29. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the graphics accelerator co-processor design of Rutman to incorporate the overlap detector implemented as a content addressable memory on a

graphics accelerator as taught by McCormack so that unacceptable data errors are avoided.

30. In regard to claim 7,

a. Rutman discloses the packet processing system of claim 5; Paragraphs 57 and 58 of the specification states that the classification or CAM processors are used to facilitate certain search and compare operations that would otherwise be computationally intensive and degrade the performance of the processor. Therefore, the examiner is taking a classification processor to be any processor that uses search and compare operations to improve system performance as stated above. Column 1, lines 11-22 of Rutman show that the co-processor of the disclosed system increases system efficiency and thus performance.

b. Rutman does not disclose wherein said co-processor is a classification processor.

c. McCormack has disclosed the use of an overlap detector implemented as a content addressable memory on a graphics accelerator chip in column 3, lines 20-39. This section also shows that values are detected (or searched for) and then compared, thus the graphics accelerator performs search and compare operations. Column 2, lines 34-36 show that an object of the invention is to avoid graphic image overlap error in digital graphic imaging, so the overlap detection is needed.

d. Mccormack has taught in column 1, lines 41-48 that overlap creates inconsistencies where incorrect data can be used causing an unacceptable error. The detection of overlap so that this error is avoided would have motivated one of ordinary

skill in the art to use overlap detector implemented as a content addressable memory as taught by McCormack in the graphic accelerator co-processor design of Rutman.

31. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the graphics accelerator co-processor design of Rutman to incorporate the overlap detector implemented as a content addressable memory on a graphics accelerator as taught by McCormack so that unacceptable data errors are avoided.

In regard to claim 16,

a. Rutman discloses the interface of claim 15, where the co-processor (P2) is a graphics accelerator as shown in figure 3.

b. Rutman does not disclose wherein said co-processor is a cont addressable memory.

c. McCormack has disclosed the use of an overlap detector implemented as a content addressable memory on a graphics accelerator chip in column 3, lines 20-39. Column 2, lines 34-36 show that an object of the invention is to avoid graphic image overlap error in digital graphic imaging, so the overlap detection is needed.

d. Mccormack has taught in column 1, lines 41-48 that overlap creates inconsistencies where incorrect data can be used causing an unacceptable error. The detection of overlap so that this error is avoided would have motivated one of ordinary skill in the art to use overlap detector implemented as a content addressable memory as taught by McCormack in the graphic accelerator co-processor design of Rutman

(thus the co-processor "is" the CAM plus other logic, which is allowed due to "is" being open ended language as opposed to "consisting of").

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the graphics accelerator co-processor design of Rutman to incorporate the overlap detector implemented as a content addressable memory on a graphics accelerator as taught by McCormack so that unacceptable data errors are avoided.

32. In regard to claim 17,

a. Rutman discloses the interface of claim 15 Paragraphs 57 and 58 of the specification states that the classification or CAM processors are used to facilitate certain search and compare operations that would otherwise be computationally intensive and degrade the performance of the processor. Therefore, the examiner is taking a classification processor to be any processor that uses search and compare operations to improve system performance as stated above. Column 1, lines 11-22 of Rutman show that the co-processor of the disclosed system increases system efficiency and thus performance.

b. Rutman does not disclose wherein said co-processor is a classification processor.

c. McCormack has disclosed the use of an overlap detector implemented as a content addressable memory on a graphics accelerator chip in column 3, lines 20-39. This section also shows that values are detected (or searched for) and then compared, thus the graphics accelerator performs search and compare operations. Column 2, lines 34-36 show that an object of the invention is to avoid graphic image overlap error

in digital graphic imaging, so the overlap detection is needed.

d. McCormack has taught in column 1, lines 41-48 that overlap creates inconsistencies where incorrect data can be used causing an unacceptable error. The detection of overlap so that this error is avoided would have motivated one of ordinary skill in the art to use the overlap detector implemented as a content addressable memory as taught by McCormack is a graphic accelerator co-processor design of Rutman.

33. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the graphics accelerator co-processor design of Rutman to incorporate the overlap detector implemented as a content addressable memory on a graphics accelerator as taught by McCormack so that unacceptable data errors are avoided.

34. In regard to claim 29,

a. Rutman discloses the method of claim 28 where said co-processor (P2) is a graphics accelerator as shown in figure 3.

b. Rutman does not disclose wherein said co-processor is a content addressable memory.

c. McCormack has disclosed the use of an overlap detector implemented as a content addressable memory on a graphics accelerator chip in column 3, lines 20-39. Column 2, lines 34-36 show that an object of the invention is to avoid graphic image overlap error in digital graphic imaging, so the overlap detection is needed.

d. McCormack has taught in column 1, lines 41-48 that overlap creates

inconsistencies where incorrect data can be used causing an unacceptable error. The detection of overlap so that this error is avoided would have motivated one of ordinary skill in the art to use the overlap detector implemented as a content addressable memory as taught by McCormack is a graphic accelerator co-processor design of Rutman (thus the co-processor "is" the CAM plus other logic, which is allowed due to "is" being open ended language as opposed to "consisting of").

35. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the graphics accelerator co-processor design of Rutman to incorporate the overlap detector implemented as a content addressable memory on a graphics accelerator as taught by McCormack so that unacceptable data errors are avoided.

36. In regard to claim 30,

a. Rutman discloses the method of claim 28; Paragraphs 57 and 58 of the specification states that the classification or CAM processors are used to facilitate certain search and compare operations that would otherwise be computationally intensive and degrade the performance of the processor. Therefore, the examiner is taking a classification processor to be any processor that uses search and compare operations to improve system performance as stated above. Column 1, lines 11-22 of Rutman show that the co-processor of the disclosed system increases system efficiency and thus performance.

b. Rutman does not disclose wherein said co-processor is a classification processor.

c. McCormack has disclosed the use of an overlap detector implemented as a content addressable memory on a graphics accelerator chip in column 3, lines 20-39. This section also shows that values are detected (or searched for) and then compared, thus the graphics accelerator performs search and compare operations. Column 2, lines 34-36 show that an object of the invention is to avoid graphic image overlap error in digital graphic imaging, so the overlap detection is needed.

d. McCormack has taught in column 1, lines 41-48 that overlap creates inconsistencies where incorrect data can be used causing an unacceptable error. The detection of overlap so that this error is avoided would have motivated one of ordinary skill in the art to use the overlap detector implemented as a content addressable memory as taught by McCormack is a graphic accelerator co-processor design of Rutman.

37. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the graphics accelerator co-processor design of Rutman to incorporate the overlap detector implemented as a content addressable memory on a graphics accelerator as taught by McCormack so that unacceptable data errors are avoided.

38. In regard to claim 37,

a. Rutman discloses the apparatus of claim 36, where said second processor (P2) is a graphics accelerator as shown in figure 3.

39. Rutman does not disclose wherein said co-processor comprises a content addressable memory.

c. McCormack has disclosed the use of an overlap detector implemented as a content addressable memory on a graphics accelerator chip in column 3, lines 20-39. Column 2, lines 34-36 show that an object of the invention is to avoid graphic image overlap error in digital graphic imaging, so the overlap detection is needed.

d. McCormack has taught in column 1, lines 41-48 that overlap creates inconsistencies where incorrect data can be used causing an unacceptable error. The detection of overlap so that this error is avoided would have motivated one of ordinary skill in the art to use the overlap detector implemented as a content addressable memory as taught by McCormack is a graphic accelerator co-processor design of Rutman.

40. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the graphics accelerator co-processor design of Rutman to incorporate the overlap detector implemented as a content addressable memory on a graphics accelerator as taught by McCormack so that unacceptable data errors are avoided.

41. In regard to claim 38,

a. Rutman discloses the apparatus of claim 36; Paragraphs 57 and 58 of the specification states that the classification or CAM processors are used to facilitate certain search and compare operations that would otherwise be computationally intensive and degrade the performance of the processor. Therefore, the examiner is taking a classification processor to be any processor that uses search and compare operations to improve system performance as stated above. Column 1, lines 11-22 of

Rutman show that the co-processor of the disclosed system increases system efficiency and thus performance.

b. Rutman does not disclose wherein said co-processor is a classification processor.

c. McCormack has disclosed the use of an overlap detector implemented as a content addressable memory on a graphics accelerator chip in column 3, lines 20-39. This section also shows that values are detected (or searched for) and then compared, thus the graphics accelerator performs search and compare operations. Column 2, lines 34-36 show that an object of the invention is to avoid graphic image overlap error in digital graphic imaging, so the overlap detection is needed.

d. McCormack has taught in column 1, lines 41-48 that overlap creates inconsistencies where incorrect data can be used causing an unacceptable error. The detection of overlap so that this error is avoided would have motivated one of ordinary skill in the art to use the overlap detector implemented as a content addressable memory as taught by McCormack is a graphic accelerator co-processor design of Rutman.

42. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the graphics accelerator co-processor design of Rutman to incorporate the overlap detector implemented as a content addressable memory on a graphics accelerator as taught by McCormack so that unacceptable data errors are avoided.

Claims 10,20,32,40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rutman and Olgiati as applied to claims 1-5, 8-9,11-15,22-28,31,34-36, and 39 above, and further in view of Prince (High Performance Memories) .

43. In regard to claim 10,

a. Rutman discloses the packet processing system of claim 1, wherein said memory comprises a dual ported random access memory. Figure 3, shows that the memory comprises a dual ported random access memory. Figure 3 shows that the memory 200 is a 3-port (with dual serial ports) VRAM, or video random access memory.

b. Rutman does not disclose that the memory is a sync-burst static memory. Appplicant has disclosed in paragraph 81 that a sync-burst static random access memory is also known as a SSRAM.

c. Prince has disclosed on pages 90-91 the design of an SSRAM chip.

d. Prince has taught on pages 2 and 18 that SSRAM technology is faster than both asynchronous SRAM technology and DRAM technology, and thus is more attractive due to the lack of wait states. This memory speed would have motivated one of ordinary skill in the art to modify the design of Rutman to use an SSRAM taught by Prince as the memory device.

44. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Rutman to use a synchronous burst (sync-burst) static random access memory as said memory so that a fast memory technology is used to boost performance as taught by Prince.

45. In regard to claim 20,

a. Rutman discloses the interface of claim 11, wherein said memory comprises a dual ported random access memory. Figure 3, shows that the memory comprises a dual ported random access memory. Figure 3 shows that the memory 200 is a 3-port (with dual serial ports) VRAM, or video random access memory.

b. Rutman does not disclose that the memory is a sync-burst static memory. Appplicant has disclosed in paragraph 81 that a sync-burst static random access memory is also known as a SSRAM.

c. Prince has disclosed on pages 90-91 the design of an SSRAM chip.

d. Prince has taught on pages 2 and 18 that SSRAM technology is faster than both asynchronous SRAM technology and DRAM technology, and thus is more attractive due to the lack of wait states. This memory speed would have motivated one of ordinary skill in the art to modify the design of Rutman to use an SSRAM taught by Prince as the memory device.

46. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Rutman to use a synchronous burst (sync-burst) static random access memory as said memory so that a fast memory technology is used to boost performance as taught by Prince.

47. In regard to claim 32,

a. Rutman discloses the method of claim 24, wherein said memory comprises a dual ported random access memory. Figure 3, shows that the memory comprises a dual ported random access memory. Figure 3 shows that the memory 200

is a 3-port (with dual serial ports) VRAM, or video random access memory.

b. Rutman does not disclose that the memory is a sync-burst static memory. Appplicant has disclosed in paragraph 81 that a sync-burst static random access memory is also known as a SSRAM.

c. Prince has disclosed on pages 90-91 the design of an SSRAM chip.

d. Prince has taught on pages 2 and 18 that SSRAM technology is faster than both asynchronous SRAM technology and DRAM technology, and thus is more attractive due to the lack of wait states. This memory speed would have motivated one of ordinary skill in the art to modify the design of Rutman to use an SSRAM taught by Prince as the memory device.

48. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Rutman to use a synchronous burst (sync-burst) static random access memory as said memory so that a fast memory technology is used to boost performance as taught by Prince.

49. In regard to claim 40,

a. Rutman discloses the apparatus of claim 34, wherein said memory comprises a dual ported random access memory. Figure 3, shows that the memory comprises a dual ported random access memory. Figure 3 shows that the memory 200 is a 3-port (with dual serial ports) VRAM, or video random access memory.

b. Rutman does not disclose that the memory is a sync-burst static memory. Appplicant has disclosed in paragraph 81 that a sync-burst static random access memory is also known as a SSRAM.

c. Prince has disclosed on pages 90-91 the design of an SSRAM chip.

d. Prince has taught on pages 2 and 18 that SSRAM technology is faster than both asynchronous SRAM technology and DRAM technology, and thus is more attractive due to the lack of wait states. This memory speed would have motivated one of ordinary skill in the art to modify the design of Rutman to use an SSRAM taught by Prince as the memory device.

50. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Rutman to use a synchronous burst (sync-burst) static random access memory as said memory so that a fast memory technology is used to boost performance as taught by Prince.

Claims 21,33,and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rutman (patent No. 5,313,586)) in view of Olgiati (patent No. 6,782,445).

51. In regard to claim 21,

a. Rutman and Olgiati discloses the interface of claim 11,

b. Rutman as applied to claim 11 does not disclose wherein said interface allows said processor to communicate with said co-processor as if said co-processor was directly connected with said processor.

c. The background of Rutman has disclosed in column 1, lines 20-22 that there are embodiments where only a bus is used as the interface for communication between processors. This would have provided direct connection between the processor and co-processor previously disclosed.

d. It is clear through inspection of the entire Rutman disclosure that using only a bus as the interface, rather than the shared memory with control logic and the bus, would use significantly less hardware and thus have a smaller area. This smaller area would have motivated one of ordinary skill in the art to modify the design of Rutman as applied to claim 11 to use only a bus as the interface between the processor and co-processor as taught by Rutman in the background.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Rutman and Olgiati as applied to claim 11 and use only a bus as the interface between the processor and coprocessor as taught by the background of Rutman so that less hardware may be used yielding a smaller area.

52. In regard to claim 33,

53. Rutman and Olgiati discloses the method of claim 24,

b. Rutman as applied to claim 24 does not disclose wherein said interface allows said processor to communicate with said co-processor as if said co-processor was directly connected with said processor.

c. The background of Rutman has disclosed in column 1, lines 20-22 that there are embodiments where only a bus is used as the interface for communication between processors. This would have provided direct connection between the processor and co-processor previously disclosed.

d. It is clear through inspection of the entire Rutman disclosure that using only a bus as the interface, rather than the shared memory with control logic and the bus, would use significantly less hardware and thus have a smaller area. This smaller

area would have motivated one of ordinary skill in the art to modify the design of Rutman as applied to claim 24 to use only a bus as the interface between the processor and co-processor as taught by Rutman in the background.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Rutman and Olgiati as applied to claim 24 and use only a bus as the interface between the processor and coprocessor as taught by the background of Rutman so that less hardware may be used yielding a smaller area.

54. In regard to claim 41,

55. Rutman and Olgiati discloses the apparatus of claim 34,

b. Rutman as applied to claim 34 does not disclose wherein said interface allows said processor to communicate with said co-processor as if said co-processor was directly connected with said processor.

c. The background of Rutman has disclosed in column 1, lines 20-22 that there are embodiments where only a bus is used as the interface for communication between processors. This would have provided direct connection between the processor and co-processor previously disclosed.

d. It is clear through inspection of the entire Rutman disclosure that using only a bus as the interface, rather than the shared memory with control logic and the bus, would use significantly less hardware and thus have a smaller area. This smaller area would have motivated one of ordinary skill in the art to modify the design of Rutman as applied to claim 34 to use only a bus as the interface between the processor and co-processor as taught by Rutman in the background.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Rutman and Olgiati as applied to claim 34 and use only a bus as the interface between the processor and coprocessor as taught by the background of Rutman so that less hardware may be used yielding a smaller area.

Applicant's arguments with respect to claims 1-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chilton (patent No. 6,317,805) disclosed a data transfer interface (e.g., see abstract).

Ales (patent No. 6,662,247) disclosed a protocol for extended data transfer in scan based industrial controller (e.g., se abstract and fig. 2).

Boucher (patent No. 6,591,302) disclosed a fast-path apparatus for receiving data corresponding to a TCP connection (e.g. se abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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EC

ERIC COLEMAN
PRIMARY EXAMINER